I CLAIM:

1. A lead frame for a semiconductor chip package, said lead frame comprising:

a frame body;

at least two chip-receiving windows formed in said frame body, each of said chip-receiving windows being adapted to receive a respective integrated circuit chip therein;

a plurality of internal connection leads formed on said frame body adjacent to said chip-receiving windows and adapted to be connected electrically to bonding pads on the integrated circuit chips in said chip-receiving windows such that internal electrical connection among the integrated circuit chips can be established via said internal connection leads; and

a plurality of external connection leads formed on said frame body adjacent to at least one of said chip-receiving windows and adapted to be connected electrically to the bonding pads on the integrated circuit chip in said at least one of said chip-receiving windows, said external connection leads serving as terminal pins such that external electrical connection with the integrated circuit chip in said at least one of said chip-receiving windows can be established via said external connection leads.

2. The lead frame of Claim 1, wherein said internal connection leads are adapted to be wire-bonded to the

bonding pads on the integrated circuit chips in said chip-receiving windows.

3. The lead frame of Claim 1, wherein said external connection leads are adapted to be wire-bonded to the bonding pads on the integrated circuit chip in said at least one of said chip-receiving windows.

4. A semiconductor chip package comprising:

a lead frame including a frame body and at least two chip-receiving windows formed in said frame body;

at least two integrated circuit chips, each of which is received in a respective one of said chip-receiving windows and has a plurality of bonding pads thereon;

a plurality of internal connection leads formed on said frame body adjacent to said chip-receiving windows, said internal connection leads being connected electrically to said bonding pads on said integrated circuit chips in said chip-receiving windows to establish internal electrical connection among said integrated circuit chips; and

a plurality of external connection leads formed on said frame body adjacent to at least one of said chip-receiving windows, said external connection leads being connected electrically to said bonding pads on said integrated circuit chip in said at least one of said chip-receiving windows, and serving as terminal pins such that external electrical connection with said integrated circuit chip in said at least one of said

chip-receiving windows is established via said external connection leads.

5. The semiconductor chip package of Claim 4, wherein said internal connection leads are wire-bonded to said bonding pads on said integrated circuit chips in said chip-receiving windows.

6. The semiconductor chip package of Claim 4, wherein said external connection leads are wire-bonded to said bonding pads on said integrated circuit chip in said at least one of said chip-receiving windows.

7. The semiconductor chip package of Claim 4, wherein said integrated circuit chip in said at least one of said chip-receiving windows is a master integrated circuit chip, and said integrated circuit chip in other ones of said chip-receiving windows is a slave integrated circuit chip.

8. The semiconductor chip package of Claim 7, wherein said master integrated circuit chip includes an embedded testing circuit for testing of said slave integrated circuit chip that is connected thereto.

9. A method of fabricating a semiconductor chip package, comprising:

forming a frame body of a lead frame with at least two chip-receiving windows, a plurality of internal connection leads adjacent to the chip-receiving windows, and a plurality of external connection leads adjacent to at least one of the chip-receiving windows;

providing at least two integrated circuit chips, and placing each of the integrated circuit chips in a respective one of the chip-receiving windows;

connecting electrically the internal connection leads to bonding pads on the integrated circuit chips in the chip-receiving windows to establish internal electrical connection among the integrated circuit chips; and

connecting electrically the external connection leads to the bonding pads on the integrated circuit chip in said at least one of the chip-receiving windows, the external connection leads serving as terminal pins such that external electrical connection with the integrated circuit chip in said at least one of the chip-receiving windows is established via the external connection leads.

10. The method of Claim 9, wherein the internal connection leads are wire-bonded to the bonding pads on the integrated circuit chips in the chip-receiving windows.

11. The method of Claim 9, wherein the external connection leads are wire-bonded to the bonding pads on the integrated circuit chip in said at least one of the chip-receiving windows.

12. The method of Claim 9, wherein the integrated circuit chip in said at least one of the chip-receiving windows is a master integrated circuit chip, and the

integrated circuit chip in other ones of the chip-receiving windows is a slave integrated circuit chip.

13. The method of Claim 12, wherein the master integrated circuit chip includes an embedded testing circuit to permit testing of the slave integrated circuit chip that is connected thereto.